UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,241	02/17/2004	Ali Keshavarzi	42P6184C	2359

8791 7590 08/08/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
NGUYEN, JOSEPH H	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,241	KESHAVARZI ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17,18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17,18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7-9, 12, 14-15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Burr (US 6,100,567).

Regarding claims 1-3, Burr discloses in figure 8 a field effect transistor comprising a substrate 810 (col. 8, line 11); a source 820 and a drain 822; an electric field terminal 852 (col. 8, line 15) in the substrate 810; and an undoped body 824 (col. 8, lines 4-5) above the electric field terminal region between the source and drain, wherein there is a barrier 808 between the electric field terminal region and the body, wherein the electric field terminal region extends partially under the source and drain, and wherein all portions of the electric field terminal region 852 have the n type material (col. 8, line 16); and the barrier 808 is an insulator layer (col. 8, line 6) between the body 824 and the electric field terminal region 852.

It is noted that region 852 is n type doped and electrically coupled to a bias contact 856, which in turn receives a bias potential for back biasing the pfet 804 (col. 8, lines 15-18). As such, region 852 can be construed as "electric field terminal region". Further, the phrase "the electric field terminal region concentrates electric fields from the

source and drain toward edges of a channel between the source and drain" is merely functional language. Element 852, which constitutes a similar structure as claimed, is capable of performing a claimed function herein.

Regarding claims 4 and 7, Burr discloses in figure 8 a field effect transistor comprising an insulator layer 808; an undoped body 824 above the insulator layer between a source 820 and a drain 822; a substrate 870 below the insulator layer; a gate 826 above the body and between the doped source and drain, the gate having a length; and an electric field terminal region 852 in the substrate, wherein the electric field terminal region extends partially under the source and drain, and wherein all portions of the electric field terminal region have the n type material (col. 8, line 16); and a channel 824 is formed in the body between the source and drain when certain voltages are applied to the source, gate and drain and the channel is undoped (col. 8, lines 4-5). Burr further discloses in figure 8 the electric field terminal region n+, which is clearly heavily doped in comparison to the doping of source and drain and comprises a different conductivity type than that of the source and drain. Further, the phrase "the electric filed terminal region concentrates electric fields from the source and drain toward edges of a channel between the source and drain" is merely functional language. Element 852, which constitutes a similar structure as claimed, is capable of performing a claimed function herein.

Regarding claim 8, since the transistor as shown in figure 8 of Burr is structurally similar to the claimed transistor, it is inherent that a threshold voltage of the Burr's transistor is set by a distance between the insulator layer and a gate insulator.

Regarding claim 9, the body 824 as shown in figure 8 of Burr has no electrical contact. As such, the body floats.

Regarding claims 12, 14-15 and 17, Burr discloses in figure 8 the electric field region 852, the substrate 810 are biased since they are coupled to a bias contact 856. Further, the electric field terminal region 852 extends essentially the entire length of the gate 826, and the transistor 804 is a pMOSFET (col. 8, line 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Houston (US 6043535) in view of Burr.

Regarding claim 20, Houston discloses in figure 3 a substrate 134 (col. 4, line 25); a source and drain 120, 122 (col. 4, lines 8-9) and a gate 116 (col. 4, line 16); a first electric field terminal region 137 (left portion of element 137) extending partially beneath the source 120 and partially beneath the gate 116, and a second electric field terminal region 137 (right portion of element 137) extending partially beneath the drain 122 and

partially beneath the gate 116; and a body 124 above the electric field terminal regions between the source and drain.

It is noted that regions 137 is part of the back gate and can be depleted (col. 6, lines 53-55). Therefore, regions 137 can function as "electric field terminal region". Further, region137, which constitutes a similar structure as claimed, is capable of performing a claimed function herein.

Houston does not disclose two transistors and an insulator layer between the substrate and body wherein the insulator layer and body each shared by the first and second field effect transistors. However, Burr discloses in figure 8 two transistors formed on the same substrate and an insulator layer 808 between the substrate 810 and body 824, and the insulator layer 808 and the body 806 are shared by the first and second field effect transistor 802, 804. In view of such teaching, it would have been obvious at the time of the present invention to modify Houston by forming two transistor on the same substrate and an insulator layer between the substrate and body wherein the insulator layer and body each shared by the first and second field effect transistors to obtain a semiconductor device in a cost effective manner since it would require less material when two transistors are formed in the same substrate.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of Wu et al. (US 5976926).

Regarding claim 5, Burr discloses in figure 8 substantially all the structure set forth in claim 5 except the electric field terminal region being doped greater than 10^{20}

cm^{-3}. However, Wu et al. discloses in figure 10 the electric field terminal region 104 being doped greater than 10^{20} cm^{-3} (col. 5, lines 63-65). In view of such teaching, it would have been obvious at the time of the present invention to modify Burr by including the electric field terminal region being doped greater than 10^{20} cm^{-3} to increase resistance between the electric field terminal region 810 and p region 810, thereby reducing leakage current.

Further, Burr and Wu et al. do not disclose the electric field terminal being p doped. However, it is well known in the art to interchange n conductivity type and p conductivity type. As such, it would have been obvious at the time of the present invention to modify Burr and Wu et al. by replacing the n type with the p type since doing so involves only routine skill in the art.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of Hwang (US 5,359,219).

Regarding claim 6, Burr discloses in figure 8 substantially all the structures set forth in the claimed invention except the body being lightly doped. However, Hwang discloses in figure 1g the body 20 being lightly doped. In view of such teaching, it would have been obvious at the time of the present invention to modify Burr by having the body being lightly doped to greatly inhibit the leakage current through thin buried oxide layers (col. 2, lines 10-13, Hwang).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of Burr (US 6,249,027).

Regarding claim 10, Burr discloses in figure 8 substantially all the structure set forth in the claimed invention except the body being biased. However, Burr discloses the body being floating (col. 1, lines 59-60). In view of such teaching, it would have been obvious at the time of the present invention to modify Burr by having the body being biased to tune the threshold voltage of a transistor (col. 1, lines 10-11).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of Kumar et al. (US 6248626).

Regarding claim 11, Burr discloses in figure 8 substantially all the structure set forth in claim 11 except the electric field terminal region floating. However, Kumar et al. discloses in figure 4D the electric field terminal region 45 floating (col. 6, line 37). In view of such teaching, it would have been obvious at the time of the present invention to modify Burr by having the electric field terminal region floating to obtain a charge storing region in a MOSFET device (col. 1, lines 36-37).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of Inoue et al. (US 6,198,134).

Regarding claim 13, Burr discloses in figure 8 substantially all the structure set forth in the claimed invention except the substrate being floating. However, Inoue et al. discloses the substrate being floating (col. 2, line 45). In view of such teaching, it would

have been obvious at the time of the present invention to modify Burr by having the substrate being floating to lower the breakdown voltage between source and drain (col. 2, lines 44-45, Inoue et al.).

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burr.

Regarding claim 18, Burr discloses in figure 8 element 804 is pMOSFET, not nMOSFET as claimed. However, it would have been obvious at the time of the present invention to modify Burr by having the nMOSFET because nMOSFET and pMOSFET are recognized in the art as equivalents.

Response to Arguments

Applicant's arguments filed 06/05/2006 have been fully considered but they are not persuasive.

With respect to claims 1, 4 and 20, applicant argues neither Burr nor Houston disclose, "the electric terminal region concentrates electric field from the source and drain toward edges of a channel between the source and drain". However, as clearly explained above, Burr discloses in figure 8 region 852 is an n type doped and electrically coupled to a bias contact 856, which in turn receives a bias potential for back biasing the pFET 804 (col. 8, lines 15-18). As such, region 852 can function as "electric field terminal region". Further, the phrase "electric field terminal region concentrates electric fields from the source and drain toward edges of a channel between the source and drain" is merely functional language. Region 852 as shown in figure 8 is between

the source 820 and drain 822, which constitutes a similar structure as claimed. Therefore, this region is inherently capable of performing the claimed function herein. On the other hand, Houston discloses in figure 3 regions 137 is part of the back gate and can be depleted (col. 6, lines 53-55). Therefore, regions 137 can function as "electric field terminal region". Further, region137, which constitutes a similar structure as claimed, is inherently capable of performing the claimed function herein.

Lastly, since the rejection of independent claims 1, 4 and 20 is proper, the rejection of dependent claims 2-3, 5-15 and 17-18 still stands.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
August 1, 2006.

KENNETH PARKER
SUPERVISORY PATENT EXAMINER